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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE THE APPLICATION OF)
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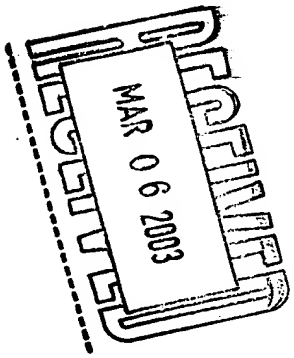
Zakwan Shaar) Group Art Unit: 2123
)
SERIAL NO: 09/761,600)
)
FILED: January 16, 2001)
)
FOR: Computer-Implemented)
Simulation Method and)
Apparatus)

INFORMATION DISCLOSURE STATEMENT



Honorable Director of
Patents and Trademarks
Washington, D.C. 20231

Dear Sir,

In accordance with the provisions of 37 C.F.R. Sections 1.97-1.98, submitted herewith is Form PTO-1449 along with copies of the five references identified therein. Also submitted herewith is a copy of the European search report in which these references were cited. This Information Disclosure Statement is timely filed and no fee is required.

GB 2219419 was cited as a category "A" document, i.e. merely of technological background interest. It describes the use of a time loop for scheduling events in a logic simulator. However, it does not contain any suggestion of the steps as recited in claim 1 of the present application.

EP 0854429 describes a digital simulation system which uses an event queue for scheduling at specified times, and a separate delta queue for scheduling changes to the state of the model that take place instantaneously. It also describes the use of process objects and signal objects to form the model. However, it does not contain any suggestion of the steps as recited in claim 1 of the present application. In particular, there is no suggestion of processing a scheduled message by calling sender and receiver processes associated with the message. Therefore, it is believed that the European Patent Office's classification of this reference as an "X" category document is clearly in error, and that it is merely technological background interest.

John B. Postel "Transmission Control Protocol" describes a protocol for transmitting messages between computers in a network. It is not concerned with simulation systems, and it cannot be seen how it is of any relevance to the present invention. In particular, there is clearly no suggestion of the steps as recited in claim 1 of the present application.

B.Lutter et al. "Using VHDL for simulation of SDL specifications" describes some aspects of the VHDL language, which is used in the preferred embodiment of the present invention. However, it clearly contains nothing relevant to the the present invention as claimed.

US 5856933 describes a system for digitally simulating an electric circuit. However, it clearly contains nothing relevant to the the present invention as claimed.

It is therefore believed that the present invention as defined in the claims is clearly patentably distinguished from these references.

Examination of the application on its merits is awaited.

Date: 2/24/03

Respectfully Submitted

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Case No.: 920190-901800
190-1468
(ICL)

Computer-Implemented Simulation Method and Apparatus

Please acknowledge receipt of the enclosed:

Serial No.: 09/761,600

Filing Date: January 16, 2001

certificate of mailing,
Information Disclosure Statement,
Information Disclosure Citation,
copies of the 5 cited references,
European Search Report,
return postcard.

Due Date (If Any):

Date Sent: February 24, 2003 kk

I hereby certify that the correspondence is being deposited with the United States Postal Service as first class mail in an envelope with sufficient postage addressed to:

Commissioner for Patents, United States Patent and Trademark Office, Washington DC 20231, on the date indicated below:

Date: February 24, 2003

BY: Kathy Kunek